Abstract of the Disclosure

Systems and methods for transferring data across clock domains in a manner that avoids metastability of the data and is very tolerant of variations in the clock signals of the different clock domains. One embodiment of the invention comprises a mechanism for passing data from a first clock to a second clock domain in a digital pulse width modulated (PWM) amplification system. In this embodiment, parallel data is generated in the process of converting PCM data to PWM data. The parallel data is processed in a clock domain having a first clock rate and is passed to a second clock domain having a clock rate that is twice the rate of the first clock domain. The parallel data is then serialized at the higher clock rate of the second clock domain.